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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/720,166

11/25/2003

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04/06/2006

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EXAMINER

WILCZEWSKI, MARY A

ART UNIT

PAPER NUMBER

2822

DATE MAILED: 04/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

.10/720,166

Applicant(s)

AHMED ET AL.

Examiner

M. Wilczewski

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 January 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 37,39-42,46-54,56 and 57 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 37,39-42,46-54,56 and 57 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This Office action is in response to the Amendment filed on January 19, 2006.

Drawings

The drawings filed on 25 November 2003 are acceptable.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 37, 39-42, 46-54, 56, and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fried et al., U.S. Patent 6,583,469; in view of Yeo et al., U.S. Patent 6,855,990; both of record.

Fried et al. disclose a semiconductor device (shown in figures 16A, 16B, 17A, 17B, 18A and 18B) which comprises a substrate 10b, an insulating layer 10u formed on the substrate, a conductive fin of silicon 12 formed on the insulating layer including a plurality of side surfaces and a top surface (Figure 18B), a source region and a drain region (regions 36 shown in Figure 18A) formed on the insulating layer and adjacent a first and second end of the fin, and a metal gate 32 formed on the insulating layer adjacent the fin in a channel region of the device (col. 6, lines 39-52, and col. 3, line 55,

Art Unit: 2822

bridging col. 4). Fried et al. disclose that gate dielectric materials such as oxides, nitrides and oxynitrides can be used, see col. 6, lines 30-40.

In column 6, lines 39-52, Fried et al. disclose that gate electrode 32 comprises any conventional conductor including metals, metal alloys, silicides and doped polysilicon. Although Fried et al. do not expressly disclose that tantalum, tantalum nitride, titanium or titanium nitride are used to form gate 32, these materials would have been obvious to one skilled in the art, since these metals and metal alloys are conventionally used in the art to form gate electrodes.

It is also noted that Fried et al. do not disclose the thickness of oxide layer 10u. However, the thickness of this layer is deemed an obvious processing parameter to be optimized by the skilled artisan. Optimization of the thickness of oxide layer 10u of Fried et al. would not require undue experimentation by one of ordinary skill in the art.

Fried et al. disclose using gate dielectric materials comprising oxide, nitride, oxynitride, or a multilayer thereof (col. 6, lines 26-38). Fried et al. lack anticipation of using a material comprising hafnium to form the gate dielectric layer. Yeo et al. discloses a semiconductor device having a fin formed of semiconductive material with an overlying gate in which the gate dielectric layer can comprise oxide, oxynitride, or a high dielectric constant material such as hafnium oxide, see figure 2 and col. 3, lines 20-39, and col. 7, lines 4-15. Since Yeo et al. teaches that an oxide, an oxynitride and a dielectric comprising hafnium can be used as gate dielectrics in a semiconductor device having a fin, it would have been obvious to one skilled in the art to substitute a material

comprising hafnium (such as hafnium oxide) for the oxide or nitride gate dielectric layer of Fried et al.

Response to Arguments

Applicant's arguments filed January 19, 2006, have been fully considered but they are not persuasive. Applicant has argued that it would not have been obvious to replace a conventional thermal growth process used to form the gate dielectric of Fried with a process that includes forming a gate dielectric that comprises hafnium. The patent of Yeo et al. is deemed a teaching of the functional equivalence of an oxide, oxynitride or hafnium-containing layer as a gate dielectric in a FinFET device, regardless of the method by which these layers are formed. Moreover, although Fried uses a conventional thermal growth process, the thicknesses disclosed by Fried et al., 0.8 to 5.0 nm (8 to 50 angstroms), are within the thickness range disclosed by Yeo et al., namely 3 to 100 angstroms. Therefore, it would have been obvious to one skilled in the art that a hafnium-containing material could have been substituted for the oxide or oxynitride gate dielectric used in the known method of Fried et al., regardless of the method used to form the hafnium-containing dielectric layer. The fact that Fried et al. teaches that the gate dielectric used in their method is formed by thermal processing would not teach away from the substitution.

Applicant has further argued that Fried et al does not teach a metal gate having a thickness in the range of 700 to 2000 angstroms. However, this is taught by Fried et al. As shown in 17b, gate electrode 32 has a thickness about equal to that of fin 12 and

Art Unit: 2822

oxide layer 16. In column 3, line 66, bridging column 4 to line 8, Fried et al. teach that fin 12 has a thickness of 300 to 200 angstroms and hard mask 14, which includes oxide layer 16, has a thickness of 100 to 1000 angstroms. Hence, the thickness of gate electrode 32 is about 400 to 3000 angstroms. This thickness range of Fried et al. clearly encompasses the claimed range of 700 to 2000 angstroms.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. Wilczewski whose telephone number is (571) 272-1849. The examiner can normally be reached on Monday and Thursday.

Art Unit: 2822

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



M. Wilczewski
Primary Examiner
Tech Center 2800